S/H front-end for two-step-channel-select low-IF receiver
Pui-In Mak; Kin-Kwan Ma; Weng-leng Mok; Chi-sam Sou; Kit-man Ho; Cheng Ng; Seng-Pan U; Martins, R.P.;
Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on , Volume: 1 , 23-26 May 2004
Pages:I-1068 - I-1071 Vol.1

[Abstract] [PDF Full-Text (618 KB)] IEEE CNF

---

6 **An IF-sampling timing skew-insensitive parallel S/H circuit**
Aho, M.; Hakkarainen, V.; Sumanen, L.; Waltari, M.; Halonen, K.;
Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on , Volume: 1 , 23-26 May 2004
Pages:I - 1052-5 Vol.1

[Abstract] [PDF Full-Text (256 KB)] IEEE CNF

---

7 **A time-multiplexed reconfigurable neuroprocessor**
Sibai, F.N.; Kulkarni, S.D.;
Micro, IEEE , Volume: 17 , Issue: 1 , Jan.-Feb. 1997
Pages:58 - 65

[Abstract] [PDF Full-Text (172 KB)] IEEE JNL

---

8 **The fat-pyramid and universal parallel computation independent of delay**
Greenberg, R.I.;
Computers, IEEE Transactions on , Volume: 43 , Issue: 12 , Dec. 1994
Pages:1358 - 1364

[Abstract] [PDF Full-Text (776 KB)] IEEE JNL

---

9 **An 8-b 85-MS/s parallel pipeline A/D converter in 1-µm CMOS**
Conroy, C.S.G.; Cline, D.W.; Gray, P.R.;
Solid-State Circuits, IEEE Journal of , Volume: 28 , Issue: 4 , April 1993
Pages:447 - 454

[Abstract] [PDF Full-Text (792 KB)] IEEE JNL

---

10 **The Balance multiprocessor system**
Thakkar, S.; Gifford, P.; Fielland, G.;
Micro, IEEE , Volume: 8 , Issue: 1 , Feb. 1988
Pages:57 - 69

[Abstract] [PDF Full-Text (1088 KB)] IEEE JNL

---

11 **A highly integrated analog baseband transceiver featuring a 12-bit 180MSPS pipelined A/D converter for multi-channel wireless LAN**
Gulati, K.; Munoz, C.; Seonghwan Cho; Manganaro, G.; Lugin, M.; Peng, M.; Pulincherry, A.; Jipeng Li; Bugeja, A.; Chandrakasan, A.; Shoemaker, D.;
VLSI Circuits, 2004. Digest of Technical Papers. 2004 Symposium on , 17-19 2004
Pages:428 - 431

[Abstract] [PDF Full-Text (455 KB)] IEEE CNF

12 **Using dynamic binary translation to fuse dependent instructions**
Hu, S.; Smith, J.E.;
Code Generation and Optimization, 2004. CGO 2004. International Symposiur on , 20-24 March 2004
Pages:213 - 224

[Abstract] [PDF Full-Text (367 KB)] IEEE CNF

13 **A deterministic globally asynchronous locally synchronous microprocessor architecture**
Heath, M.; Harris, I.;
Microprocessor Test and Verification: Common Challenges and Solutions, 200: Proceedings. 4th International Workshop on , 29-30 May 2003
Pages:119 - 124

[Abstract] [PDF Full-Text (265 KB)] IEEE CNF

14 **Performance evaluation of a demand assignment multiple access scheme for mobile radio dispatch over satellite**
Powell, C.J.; Leung, V.C.M.;
Communications, Computers and Signal Processing, 1991., IEEE Pacific Rim Conference on , 9-10 May 1991
Pages:418 - 421 vol.2

[Abstract] [PDF Full-Text (396 KB)] IEEE CNF

h eee e eee g e ch e ch e e c e e e c e